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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,293	08/27/2003	Hedley James Francis	550-450	4462

23117 7590 05/13/2009

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
05/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,293	FRANCIS ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-62 have been examined.

Acknowledgement of papers filed: appeal brief on 30 May 2008. These papers filed have been placed on record.

In view of the appeal brief filed on 30 May 2009, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below. To avoid abandonment of the application, appellant must exercise one of the following two options: (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or, (2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid. A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 43-62 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The program product is treated like an article

of manufacture. Therefore, the disclosed storage medium encoded with instruction code appears to be acceptable. However the following portion of claim 43 is problematic: "said computer program produce comprising: code configured..." It is not clear to which code the language is referring or whether that code is included on a storage medium. Examiner suggests changing the language "said computer program product comprising" to "said instruction code comprising."

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-17, 21-38, 42-58, and 62 rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima (5,598,544) in view of Watt (5,802,598).

3. As to claim 1,22,43, 43, Ohshima disclosed at least: a) detecting an attempt to execute a variable length instruction spanning two discrete memory address regions (see fig.7A), the two discrete memory address regions (see the basic segment 1 and basic segment 2) being a current memory address region and a following memory address region (see also fig. 515 to see how pointer P was used to address leading end of segment in the memory 403); b) concatenating instruction data from an end portion of

the current memory address region and a start portion of following memory address region into a fix-up memory address region of said memory (see the read out position by pointer P in co1.2, lines 38-50) to form concatenated instruction data containing said variable length instruction (instruction code unit length, see also the concatenation of instruction fields in fig.1 and fig.5, see also fig.7B, Ohshima's warp-around feature was a concatenation);

c) diverting program execution flow to execute the current variable length instruction from within the concatenated instruction data in the fix-up memory address region (see the execution unit 13 in fig.4 and fig.8C, for fixed up address see rearranged P pointer); and (d) restoring program execution flow to execute instructions (execution not explicitly shown, but see execution unit [13] in 4) following the variable length instruction from within following memory address region (see next instruction segment in the memory region [404] in fig.5). 4. Ohshima did not specifically teach the triggering of the memory abort as claimed. However, Watt taught bits of variable size subsection from the address space were set to cause a memory abort generator to generate a memory abort signal. (co1.4, lines 45-53). It would have been obvious to one of ordinary skill in the art to use Watt in Ohshima for triggering the memory abort as claimed because the sue of Watt could provide Ohshima the ability to preserve a particular memory range, thereby avoiding the data loss due to improper memory address space access. And, it could be implemented by predefining the abort Signal of Watt in Ohshima with modified system variables (e.g. the specific type of abort signal for read and write), so that memory abort of Watt could be recognized by Ohshima, and because

Ohshima also taught that execute a variable length instruction spanning two discrete memory address regions (see fig.7A), the two discrete memory address regions, see the basic segment 1 and basic segment 2, see also fig. 515 to see how pointer P was used to address leading end of segment in the memory 403), which was a suggestion of the need for including an indication or a signal for memory abort due to the access to wrong memory address regions likely to occur, and for the above reasons, provided a motivation. 11. As to the remarks regarding the fix-up memory address region and Ohshima's code bus, see rearranged P pointer as a fixed up address in fig.4 and fig.8C). The address pointer defined the address region. See also fig.2a,b for fix up memory region. 5. As applicant's remark that decoding always takes place from Ohshima's instruction code bus, as result there is no need for divert program execution, examiner would like to point out that the fact that decoding always takes place, it does not necessarily mean that execution can be diverted. Execution can be diverted even after decoding.

4. As to claim 22, claim 2 is directed to the same scope as claim 1 in apparatus.

5. As to claim 43, claim is directed the same scope as claim 1 in program product format. The examiner holds that this program product is not given a patentable weight because no specific recitation in the body of the claim reflects the specific elements of the program product.

6. As to claim 2,23, Ohshima also included hardware control (see fig.11).

7. As to claim 3, 24, Ohshima also included software control (see micro ROM control in co1.7, lines 40-42, see also PLA).

8. As to claims.4,25,45, 46, the structural relation between the memory and the instruction buffer has been reflected into the claim, therefore, Ohshima also included instruction buffer (see the instruction buffer in fig.6A, this instruction buffer include the instruction storage 403, see also readout buffer at the output of storage 3 in fig.7B).

9. As to claims 5,26,47, see instruction fetched from the memory [430] to an instruction buffer [instruction register] before being executed in fig.4).

10. As to claims 6,27, Ohshima also included sequential addresses (see the entry 404 404' 404").

11. As to claims 7,8,27,28,29, 48,49, Ohshima also marked the valid instruction (see the marking for indicate whether to simultaneously decode the segments in co1.7, lines 54-65, co1.10, lines 28-48).

12. As to claims 9, 30, 50, Ohshima also disclosed a program counter (see program counter in co1.2, lines 41-43). 19. As to claims 10,31,51, see how the program counter P readjusted to the leading position in co1.8, lines 10-53).

13. As to claims 11,12, 13, 14,32,33,34, 35,52,53,54, 55, for the flag for single variable instruction length, see the instruction unit length in co1.2, lines 48-50, see the L in the position identifying circuit in co1.15, lines 56-58, co1.16, lines 1-9).

14. As to claims 16,17, 36,37,38, 56, 57, 58, Ohshima also to point to the next instruction following the current instruction (see. how the use of pointer 7 to point each of the 7 fields in a given entry 4 in co1.8, lines 10-23, for calculation, see calculation of

address in col., lines 40-54 for background). AS to the diversion, it is read as pointer action (see the pointer P of Ohshima).

15. As to claims 21,42, 62, see instruction storage 403 in fig.4.

16. As to claims 18-20,39-41,59-61, limitations of parent claims 1,22,43 have been discussed above, therefore, will not be repeated herein. Neither Ohshima nor Watt specifically taught the java byte code as claimed. However, Komatsu disclosed a java byte code of variable length (see co1.1, lines 56-60). It would have been obvious to use the java by code as claimed because the use of Komatsu could provide Ohshima the ability to process his variable length instruction in a different type of language, such as the by codes, or like, and therefore, increasing the control adaptability of Ohshima, and because Ohshima already taught the rearrangement of his variable length instruction fields, one of ordinary skill in the art should be able to recognize the applicability of petitionable program codes, such as the byte codes, which was already taught by Komatsu to be used in a variable length instruction, into Ohshima in order to enhance the system compatibilities, and for doing so, provide a motivation.

17. As to the further instruction set in claim 19, Komatsu also included a further instruction set (see C++ programming in co1.1, lines 30-35).

18. As to the branch in claim 20, Ohshima already taught branch (see jump in co1.7, lines 54-65).

Response to Arguments

Applicant's arguments with respect to prior art rejections have been considered but are moot in view of the new ground(s) of rejection. The section 101 rejection has been amended.

A. 101 rejection of 43-62

The previous section 101 rejection has been amended to comply with current law.

B. Art Rejection

1. No "fix-up memory"

Appellant argues that there is no fix-up memory because the extended portion of the instruction in Ohshima is concatenated in a bus, which is not a memory. Examiner disagrees. In 7A it is clear that the basic segments and expanded portions are both physically and conceptually concatenated prior to being fetched on a bus. Therefore, this is the "fix-up memory" as claimed.

2. No diverting

Applicant states:

> The Examiner maps the claimed diverting and restoring to execution of an instruction on Ohshima's instruction code bus and execution of the next instruction. But the instruction code bus is not part of the memory address space. Also, instruction decoding always takes place from Ohshima's instruction code bus (see Fig. 1). So there is no need to divert program execution flow to the instruction code bus or restore program execution flow from the instruction code bus.

Examiner disagrees. The claim language is as follows:

> Diverting code encoded in the storage medium which, when executed by the data processing apparatus, controls the data processing apparatus to divert program execution flow to execute said current variable length instruction within said concatenated instruction data in said fix-up memory address region;

The word "diverting" implies that there is a typical program flow execution and that this execution is somewhat altered on the basis of the variable length instruction. Ohshima discloses this limitation. Indeed, Appellant plainly admits that the fetching and decoding are different when an extended length instruction is used (Appeal Brief pages 13-14).

Applicant's argument appears to hinge on the fact that the diversion does not occur from a memory location, which in turn hinges on whether figure 7A of Ohshima can be considered a "fix-up memory." As indicated in B(1) above, the fix-up memory is found in figure 7A of Ohshima. Knowing that, Appellant's argument is largely moot.

3. Modification of Ohshima is Insufficient

Applicant makes the statement: "There is no concern of improper memory access in Ohshima" (Appeal Brief page 16). It is unclear how Appellant comes to this conclusion. There is an addressable extended memory region in Ohshima 7A which would be improper if accessed directly. An abort signal would be a simple and efficient way to solve this problem. Therefore, the rejection under section 103 appears to be proper.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRIAN P. JOHNSON whose telephone number is (571)272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Brian Johnson/ Patent Examiner, Art Unit 2183